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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/597,996	08/15/2006	Radu Catalin Surdeanu	NL04 0166 US1	8935

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NXP, B.V.
NXP INTELLECTUAL PROPERTY & LICENSING
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
TRAN, TRANG Q	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/597,996	SURDEANU ET AL.	
	Examiner	Art Unit	
	TRAN TRAN	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-10,12 and 14-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-10,12,14-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, and 5-10, 12, 14-16, 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over En et al. (US 6,441,433) in view of Krivokapic (US 6,888,198).

Re. claim 1, En discloses in Fig. 1 and related text a semiconductor device comprising a silicon-containing semiconductor body (SOI-13) with a surface, which semiconductor body is provided, near the surface thereof, with a transistor comprising: a gate (36) situated at the surface and having a side wall spacer (58) on either side of the gate (see Fig. 1), and further comprising, on either side of the gate (36), a diffusion region (24/28/50) formed in the semiconductor body, at least one diffusion region (24/28/50) being provided at the surface of the semiconductor body with a silicide region (46/48/54), characterized in that the silicide region (46/48/54) extends along the surface of the semiconductor body and continues under the side wall spacer (46/48/54).

wherein the side wall spacer (58) has a shaped (see Fig. 1) and comprises a first portion (right portion), which borders on the gate and extends substantially perpendicularly with respect to the surface of the semiconductor body, and a second portion (left portion) which extends along the surface of the semiconductor body (see

Fig. 1), wherein the silicide region (46/48/54) is completely below the side wall spacer (58), wherein the side wall spacer (58) is configured to directly contact the entire surface of a side of the gate (36), and wherein the side wall spacer (58) is made of one material (silicon dioxide or silicon nitride, see Col. 5 lines 31-35).

En does not explicitly disclose a silicide region continues for more than 10 nm under the side wall spacer and a side wall spacer is L-shaped.

Fig. 1 of Krivokapic teaches it is known in the art to provide a side wall spacer (48) is L-shaped.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the silicide region continues for more than 10 nm under the side wall spacer and the L-shape of the side wall, as taught by Krivokapic in En, in order to reduce resistance and to protect the gate.

Futhermore, it has been held that discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233; *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980); *In re Huang*, 100 F.3d 135, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996).

Furthermore, the shape of the side wall spacer was a matter of choice which a person of ordinary skill in the art would have found obvious absent persuasive evidence that the particular configuration of the side wall spacer was significant. See *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Re. claim 2, En and Krivokapic disclose the semiconductor device as claimed in claim 1, En further discloses characterized in that the silicide region (46/48/54) contains a metal (see col. 3 lines 56-66) which, in the silicide region formed, has a higher diffusion rate than silicon (En teaches the silicide region has the same material as claimed invention; therefore it has higher diffusion rate than silicon, see claim 3 below for claimed material).

Re. claim 3, En and Krivokapic disclose the semiconductor device as claimed in claim 2, En further discloses characterized in that the metal is selected from the group comprising nickel (Ni) (see col. 3 lines 56-66).

Re. claims 5 and 19, En and Krivokapic disclose teaches semiconductor device as claimed in claim 1, however En and Krivokapic may not explicitly teach a second portion of the L-shaped side wall spacer has a thickness, measured in a direction perpendicular to the surface of the semiconductor body, of 5 to 20 nm (maximally 40 nm).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the second portion of the L-shaped side wall spacer has a thickness, measured in a direction perpendicular to the surface of the semiconductor body, of maximally 40 nm, in order to optimize the performance of the device.

Futhermore, it has been held that discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233; *In re Boesch*, 617 F.2d

272, 205 USPQ 215 (CCPA 1980); *In re Huang*, 100 F.3d 135, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996).

Re. claim 6, En and Krivokapic disclose the semiconductor device as claimed in claim 1, characterized in that an insulating layer (14) extends in the semiconductor body (13) in a direction parallel to the surface of the semiconductor body (13, as seen in fig. 1).

Re. claims 7-8, En and Krivokapic disclose the semiconductor device as claimed in claim 1, however En and Krivokapic may not explicitly teach whereas Fig. 1 and Col 2, lines 14-15 of Krivokapic discloses characterized in that the semiconductor body comprises a germanium component or strained-silicon layer (as seen in Col 2, lines 14-15).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the semiconductor body comprises a germanium component or strained-silicon layer of Krivokapic in En, in order to improve the performance of the device.

Re. claim 9, En and Krivokapic disclose the semiconductor device as claimed in claim 1, En further discloses characterized in that the at least one diffusion region (24/28/50) comprises the silicide region (46/48/54) as seen in Figs. 2A-2D.

Re. claim 10, En and Krivokapic disclose discloses the semiconductor device as claimed in claim 1, En further discloses characterized in that the at least one diffusion region (24/50/28) comprises a diffusion region extension (extension implant region 50/28), the silicide region (46/48/54) comprising a silicide region extension (48/54), the silicide region extension falling completely within the diffusion region extension (50/28).

Re. claim 11, En and Krivokapic disclose the semiconductor device as claimed in claim 1, En further discloses characterized in that the silicide region (46/48/54) is completely below the side wall spacer (58).

Re. claim 12, En and Krivokapic disclose the semiconductor device as claimed in claim 2, however En and Krivokapic disclose may not explicitly teach whereas Fig. 2 and ¶28 of Yang discloses characterized in that the silicide layer (260) comprising metal which is palladium (Pd).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the silicide layer having claimed material, in order for suitable material use.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide claimed material for silicide layer, since it have been held to be within the general skill of a worker in the art to select a know material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416

Re. claim 14, En and Krivokapic disclose discloses the semiconductor device as claimed in claim 1, En further discloses semiconductor device as claimed in claim 1, wherein the side wall spacer (58) is configured to contact the entire surface of a side of the gate (36) without an intervening structure (see Fig. 1).

Re. claim 15, En and Krivokapic disclose discloses the semiconductor device as claimed in claim 1, En further discloses an insulation layer (32) that is located below the gate (36), wherein the side wall spacer (58) is configured to directly contact the insulation layer (32).

Re. claims 16 and 18, En and Krivokapic disclose discloses the semiconductor device as claimed in claim 1, En further discloses an insulation layer (32) that is located below the gate (36), wherein the gate (36) comprises a conductive layer that is made of polycrystalline silicon (Col. 5, lines 5-8) and a silicide layer (56), and wherein the side wall spacer (58) is configured to directly contact the insulation layer (32), the conductive layer and the silicide layer (as seen in Fig. 1).

Re. claim 20, En and Krivokapic disclose discloses the semiconductor device as claimed in claim 1, En further discloses the silicide region (58) contains a metal (see col. 3 lines 56-66) which, in the silicide region formed, has a higher diffusion rate than silicon

(En teaches the silicide region has the same material as claimed invention; therefore it has higher diffusion rate than silicon, see claim 3 above for claimed material).

En and Krivokapic do not disclose wherein the second portion of the L-shaped side wall spacer has a thickness, measured in a direction perpendicular to the surface of the semiconductor body, of maximally 40 nm.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to include wherein the second portion of the L-shaped side wall spacer has a thickness, measured in a direction perpendicular to the surface of the semiconductor body, of maximally 40 nm in the combined device, in order to optimize the performance of the device.

Furthermore, it has been held that where then general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

Re. claim 21, En and Krivokapic disclose discloses the semiconductor device as claimed in claim 1, En further discloses the silicide region (58) contains a metal (see col. 3 lines 56-66) which, in the silicide region formed, has a higher diffusion rate than silicon (En teaches the silicide region has the same material as claimed invention; therefore it has higher diffusion rate than silicon, see claim 3 above for claimed material), and wherein an insulating layer (14) extends in the semiconductor body in a direction parallel to the surface of the semiconductor body (13, as seen in Fig. 1).

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over En in view of Krivokapic as applied to claims above, and further in view of Pellerin et al. (WO 02/075781A2 as disclosed in the IDS).

Re. claim 17, En and Krivokapic disclose discloses the semiconductor device as claimed in claim 1, En further discloses comprising an insulation layer (32) that is located below the gate (36), wherein the gate comprises conductive layer, and wherein the side wall spacer (58) is configured to directly contact the insulation layer and the metal conductive layer (as seen in Fig. 1).

En discloses a gate (46) comprises a metal conductive layer (pg. 4, line 14).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the gate comprises a metal conductive layer of Pellerin in En, in order for suitable material use.

Response to Arguments

Applicant's response filed on 03/31/2011 is acknowledged and is answered as follows.

Applicant's arguments, see pg. 3, with respect to the rejection that En et al. do not teach the limitation "the silicide region extends along the surface of the semiconductor body and continues for more than 10 nm under the side wall spacer" have been fully considered but they are not persuasive in view of the following reasons.

En et al. clearly disclose in Fig. 1 and the related text the silicide region extends along the surface of the semiconductor body 12/13/14 and continues under the side wall spacer 58.

En et al. may not explicitly disclose the silicide region continues for more than 10 nm under the side wall spacer.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the silicide region continues for more than 10 nm under the side wall spacer, in order to optimize the performance of the device. Futhermore, it has been held that discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233; *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980); *In re Huang*, 100 F.3d 135, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996).

However, there is no evidence indicating the dimension are critical and it has been held that it is not inventive to discover the optimum or workable range of a result-effective variable within given prior art conditions by routine experimentation. See MPEP *§* 2144.05.

According to MPEP § 2144.04(IV)(A): In *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

Applicant's arguments, see pg. 3, with respect to the rejection that En et al. do not teach the limitation "the side wall spacer is L-shaped"

Applicant does not claim the material of the spacer. For the broadest interpretation, the spacer can be (arbitrarily chosen) any layer adjacent or on the sidewall of the gate electrode. Therefore, En et al. in view of the Krivokapic et al. disclose the side wall spacer is L-shape.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the spacer has L-shape in En et al., order to achieve the device properties.

Furthermore, the change in shape of the shape of the spacer was a matter of choice which a person of ordinary skill in the art would have found obvious absent persuasive evidence that the particular configuration of the spacer was significant. See *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

According to M.P.E.P. § 2144.04(IV)(B), the court held that the configuration of the claimed disposable plastic nursing container was a matter of choice which a person of ordinary skill in the art would have found obvious absent persuasive evidence that the particular configuration of the claimed container was significant. See *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

In Dailey, the court stated that "[a]ppellants have presented no argument which convinces us that the particular configuration of their container is significant or is anything more than one of numerous configurations a person of ordinary skill in the art would find obvious" (357 F.2d at 672-73, 149 USPQ at 50).

In the instant case, Applicant is claiming towards the spacer where the shape is manipulated. Prior art teaches the spacer, wherein they are similar, but only the shape is different. Therefore, it is unpatentable by a mere change in shape for which one of ordinary skill in the art would have found obvious.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the size, shape and layout of the protrusions) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181,26 USPQ2d 1057 (Fed. Cir. 1993).

In view of the foregoing reasons, the Examiner believes that all Applicant's arguments and remarks are addressed. The Examiner has determined that the previous Office Action is still proper based on the above responses. Therefore, the rejections are sustained and maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRAN TRAN whose telephone number is (571)270-3259. The examiner can normally be reached on Mon - Thu (9am-5pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T. Q. T./
Examiner, Art Unit 2811
/CUONG Q NGUYEN/
Primary Examiner, Art Unit 2811